Session 24 Overview

High-Performance Digital Circuits

Chair: David Blaauw, University of Michigan, Ann Arbor, MI

Associate Chair: Masayuki Mizuno, NEC, Kanagawa, Japan

With the introduction of 65nm technology, the scaling roadmap for CMOS shows no signs of slowing down. With each new technology node, previously unattainable performance levels come within reach for processor designers. However, every new technology node also brings new challenges for the circuit designers to achieve these performance gains while maintaining robust and reliable designs. Subthreshold and gate leakage currents have become dominant issues in the life of designers. Process and environmental variations have emerged as new critical issues that must be addressed up front in today's design efforts. This session includes seven papers that address new high-performance circuit techniques for robust processor designs. The papers address arithmetic designs, a register-file design, intra-chip communication, and dynamic and static circuit structures.

The first three papers focus on new arithmetic designs, which form the heart of high performance processors. The authors of Paper 24.1 present new 64b fixed-point and floating-point execution units for the POWER6™ processor implemented in 65nm CMOS. The design sets a new benchmark with over 4GHz performance and a latency of 13 FO4 delays for the fixed-point unit and 91 FO4 delays for the double-precision floating-point unit. In Paper 24.2, a trade-off study of different 64b adder designs is described; a sparse radix-4 Ling parallel prefix tree architecture is selected as the optimal design. The proposed adder is implemented in 90nm CMOS with a 250ps cycle time and 311mW measured power consumption. A new implementation of a 64b adder using the recently proposed output-prediction logic (OPL) is discussed in Paper 24.3. This aggressive dynamic logic circuit family is enhanced with self-calibrating local clock generation using dual-rail completion detection. The adder design has a cycle time of 238ps in 0.13μm CMOS and shows a speed improvement of 1.8× over a domino-logic implementation.

A new keeper circuit for dynamic domino gate structures with wide AND-OR evaluation trees is the focus of Paper 24.4. In this design, the keeper strength is dynamically adjusted through a replicated evaluation tree leakage path and current mirror. The new technique compensates for process, temperature and voltage variations and is demonstrated in a 72×1024 3-write/4-read SRAM design in 90nm CMOS.

The authors of Paper 24.5 focus on data synchronization for large global on-chip signals, which has become a difficult issue in high-frequency processor designs. A new latency-insensitive synchronization method using FIFO queues is implemented in 0.18μm CMOS for a 5.4mm bus supporting a bandwidth of 3Gb/s per wire and demonstrates compensation for ±2 clock cycles of data-clock skew.

In Paper 24.6, a fast dynamic 14:1 MUX flip-flop, implemented in 90nm CMOS technology, is described. The circuit uses replication to obtain state retention when all select signals are inactive. This structure achieves a measured clock-Q delay of less than 250ps with a 1.2V supply.

We round out the session with Paper 24.7, in which a new 8.8GHz 16×64b register-file design implemented in 65nm CMOS is presented. The design has a power consumption of 198mW with 25mW active leakage and can achieve 10.1GHz single-cycle read/write at 1.4V. Particular attention is paid to process variation through the use of variation-tolerant keeper compensation. Leakage current is addressed through the use of a leakage-tolerant bitline/wordline architecture and the use of non-minimal channel lengths.

 1-4244-0079-1/06/$20.00 ©2006 IEEE

24.1 4GHz+ Low-Latency Fixed-Point and Binary Floating-Point Execution Units for the POWER6 Processor **8:30 AM**
B. Curran, IBM, Poughkeepsie, NY

A 1-pipe stage, low-latency, 13 FO4, 64b fixed-point execution unit, implemented in a 65nm SOI CMOS process, allows back-to-back execution of data dependent adds, subtracts, compares, shifts, rotates, and logical operations. A 7-pipe stage, 91 FO4, double-precision floating-point unit allows forwarding of dependent results after 6 cycles in most cases.

24.2 A 250ps 64b Carry-Lookahead Adder in 90nm CMOS **9:00 AM**
S. Kao, University of California, Berkeley, CA and Xilinx, San Jose, CA

A 64b adder with a single-execution cycle time of 250ps is fabricated in a 90nm CMOS technology. The adder is designed using an energy-delay optimization framework that can rapidly optimize different microarchitectures in the energy-delay space. The microarchitecture with the lowest delay, a sparse radix-4 Ling parallel prefix tree, is chosen. The carry tree uses footless domino logic to minimize delay while the non-critical paths use minimum-size static logic to reduce energy. The adder consumes 311mW from a 1V supply.

24.3 A 64b Adder Using Self-Calibrating Differential Output Prediction Logic **9:30 AM**
C. Sechen, University of Washington, Seattle, WA

A 64b adder based on self-calibrating differential output-prediction logic is fabricated in a 0.13µm 1.2V process. It has a normalized worst-case delay of 238ps (3.9 FO4 inverter delays) and consumes 30pJ per operation, which is 1.8X faster and 2X lower in energy than previously published 64b adder results, which were based on domino logic.

24.4 A Leakage Current Replica Keeper for Dynamic Circuits **10:15 AM**
N. Tzartzanis, Fujitsu Laboratories of America, Sunnyvale, CA

A 1T-overhead keeper circuit for dynamic gates replicates the evaluation stack leakage current and thus provides PVT tracking. Implemented in a 90nm CMOS process, the keeper enables design of AND-OR circuits with 30% more legs; 16 to 24 leg dynamic AND-OR circuits are 25 to 40% faster than those with a conventional keeper at the same noise margin. The circuit operation is verified on a 72×1024 3W/4R SRAM.

24.5 An On-Chip Delay- and Skew-Insensitive Multi-Cycle Communication Scheme **10:45 AM**
P. Caputa, Linköping University, Linköping, Sweden

A synchronous latency-insensitive design (SLID) method that mitigates unknown on-chip global wire delays and removes the need for controlling global clock skew is presented. An SLID-based 5.4mm-long on-chip global bus, fabricated in a standard 0.18µm CMOS process, supports 3Gb/s/wire and accepts ±2 clock cycles of data-clock skew.

24.6 A 14:1 Dynamic MUX FF with Select Activity Detection **11:15 AM**
M. Sumita, Matsushita, Nagaokakyo, Japan

A 14:1 dynamic MUX FF is discussed. The design uses 2 cascaded dynamic stages to investigate the 14:1 MUX with a dynamic FF. In addition, replication is used to maintain latch state when all selects are inactive. The timing of the MUX FF is evaluated with a proposed slew detector. Fabricated in a 90nm CMOS process, the chip has a 2× speed increase and 70% area reduction compared to conventional methods.

24.7 An 8.8GHz 198mW 16x64b 1R/1W Variation-Tolerant Register File in 65nm CMOS **11:45 AM**
S. Hsu, Intel, Hillsboro, OR

A 16×64b 1R/1W register file is fabricated in 65nm CMOS technology. The 0.017mm^2 chip performs 8.8GHz fused decode and read/write operations in a single cycle while dissipating 198mW at 1.2V, 50°C, with frequency scalable to 10.1GHz at 1.4V, 50°C. Variation-tolerant keeper compensation, leakage-tolerant BL/WL architecture and optimal non-minimum channel-length usage enable wide PVT operating range with an active leakage of 25mW and a BL noise droop ≤8mV.